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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/700,464	11/15/2000	Terunao Hanaoka	107284	5910

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EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/700,464	HANAOKA ET AL.	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13-17,20-36 and 39-49* is/are pending in the application.

4a) Of the above claim(s) *25-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13-17,20-24 and 39-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgment

1. The amendment filed on 12/02/2003 n response to the Office action mailed on 09/03/2003 has been entered. The present Office action is made with all the suggested amendments being fully considered.

Election/Restrictions

2. Claims 25-36 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.

Claim Rejections - 35 USC § 112

3. Claims 13, 22 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification as originally filed does not disclose that the uppermost layer of the insulating layers (i.e. top single layer) has protrusions and depression. Note that the protrusions and depression are formed by the plurality of layers and not by a single layer.

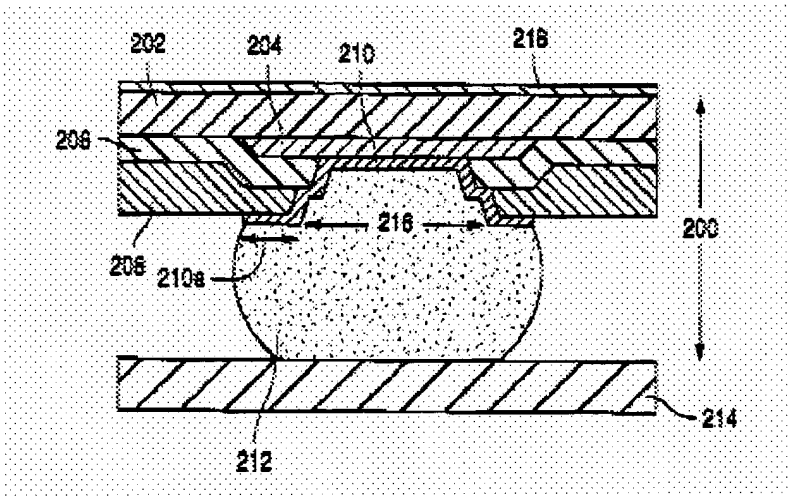
Claim Rejections - 35 USC § 103

4. Claims 1-9, 13-17, 21-24 and 39-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (6,075,290) in view of Elenius et al. (US 6,441,487).

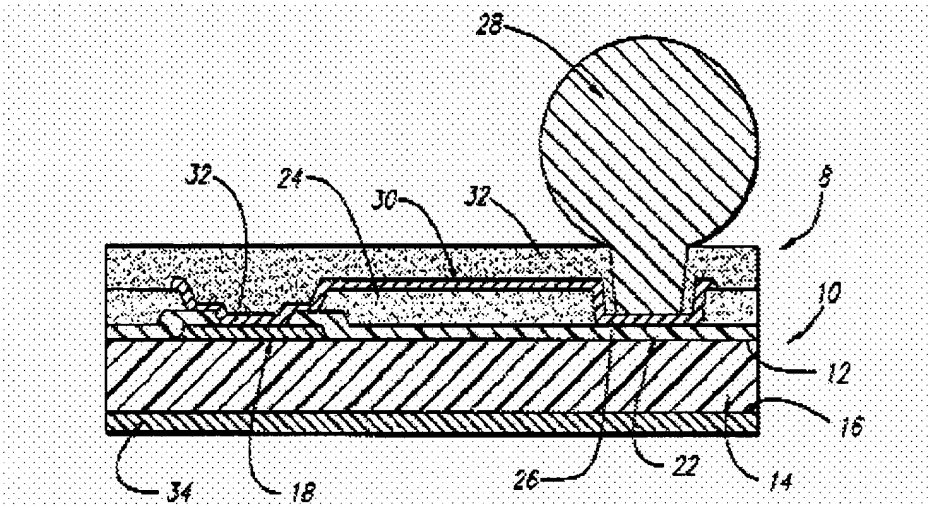
5. Regarding claims 1, 21, 23, 39, 48 and 49, Schaefer (e.g. fig. 2) shows an electronic instrument having a circuit board 214 in which a semiconductor device comprising:

- A semiconductor element 202 having a plurality of electrodes 204;
- An interconnect pattern (210) electrically connected to the electrodes;
- And external terminals 212 electrically connected to the interconnect pattern.

6. Schaefer shows a plurality of insulating or passivation layers 206/208 formed around the external terminals on the interconnect pattern. As shown in figure 2, each of the insulating layers has a hole that includes an opening portion. The external terminals are positioned in the opening portions that have one-step portion formed on the inside surface. The insulating layers include a first 208 and a second layer 206. The coefficient of thermal expansion of the first layer which is made of BCB is greater than the coefficient of thermal expansion of the second layer which is made of silicon oxide (inherent property of the material, col. 5/ll. 59-col. 6/ll. 14). The Young's modulus expansion of the second layer which is made of silicon oxide is greater than the Young's modulus of the first layer which is made of BOB (inherent property of the material, col. 5/ll. 59-col. 6/ll. 14). Schaefer, however, shows that external terminals overlap the electrodes.



7. Elenius (e.g. figs. 1 and 2) shows a semiconductor device including a semiconductor element 14 having external terminals 28 electrically connected to a interconnect pattern 30 without overlapping electrodes 18. According to Elenius this type of embodiment provides an improved chip scale package that has a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit (col. 3/lls. 16-41). Elenius discloses that the size and the amount of the solder bumps are compromised due to the fact that the solder pads are typically located at the perimeter of the integrated circuit. Elenius discloses that the solder bump contact pads can be redistributed internally, away form the outer perimeter of the integrated circuit; the size of such solder bumps is unchanged. Therefore, the requirements of complex integrated circuits can be fulfilled (col. 2/lls. 25-40).



It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically connect the interconnect the patterns and the external terminals disclosed by Schaefer without overlapping the electrodes in order to provide an improved chip scale package having a small form factor, i.e. the resulting chip scale package is not larger than the size of the original integrated circuit, and to internally redistribute the solder bump contact pads, away form the outer perimeter of the integrated circuit, in order to fulfill the requirements of complex integrated circuit as taught by as taught by Elenius.

8. Regarding claims 2 and 40, Schaefer shows that the one of the plurality of insulating layers has a stress relieving function (inherent property of the material, col. 6/lls. 1-14).

9. Regarding claims 3 and 41, Schaefer shows that one of the plurality of insulating layers is formed of a resin e.g. polyimide (col. 6/lls. 1-14).

10. Regarding claims 4 and 42, Schaefer shows that the insulating layers contact the external terminals at opening portions each of which has an inclined surface providing a taper increasing in size from the second layer to the first layer.

11. Regarding claims 5 and 43, Schaefer shows that each of the external terminals includes a base and a connection portion provide on the base. Also, the base is provided in an opening portion through which each of the external terminals contact the insulating layers.

12. Regarding claims 6 and 44, Schaefer shows that the insulating layers contact the external terminals at opening portions each of which is formed with a curved surface.

13. Regarding claims 7 and 45, Schaefer in view of Elenius shows that the interconnect pattern is formed on the layer 208 which is below the plurality of insulating layers. In reference to the claim language referring to stress relieving function, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). In any case, Schaefer shows that the interconnect pattern is formed on a stress relieving layer formed below the plurality of insulating layers (col. 6/lls. 1-14).

14. Regarding claims 8 and 46, Schaefer shows that the uppermost layer of the insulating layers is formed over the whole surface of the second layer of the insulating layers from the uppermost layer except for an area of the external terminal.

15. Regarding claim 9 and 47, Schaefer shows that the uppermost layer of the insulating layers has its area smaller than an area of a just under the uppermost layer.

16. Regarding claims 13, 22 and 24 (as understood), Schaefer shows that the interconnect patter is formed on the uppermost layer 208 of the insulating layers that form profusions and depression. The external terminal is formed in the depression.

17. Regarding claim 14, Schaefer shows that the insulating layers have a stress relieving function (col. 6/ll.s 1-14).

18. Regarding claim 15, Schaefer shows that the insulating layers comprises a resin (col. 6/lls. 1-14).

19. Regarding claim 16, Schaefer shows that the external terminals includes a base and a connection portion provided on the base. The base and the interconnect pattern are constructed as a single member.

20. Regarding claim 17, Schaefer shows that the depressions are formed to have an opening extremity lager than the bottom.

21. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schaefer et al. (6,075,290) in view of Elenius et al. (US 6,441,487) further in view of Kitayama et al. (US 5744382).

22. Regarding claim 20, Schaefer in view of Elenius shows most aspects of the instant invention (see comments above). However, Schaefer in view of Elenius does

not disclose a protective film formed on the uppermost layer of the semiconductor device. Kitayama (e.g. fig. 7) shows a semiconductor device having a protective film 4 formed on its uppermost layer. Also, Kitayama discloses that the protective layer is used to protect the device electronic components against oxidation and moisture (col. 4/lls. 3-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a protective film on the upper most layer of the semiconductor device disclosed by Schaefer in view of Elenius to protect its electronic components against oxidation and moisture as suggested by Kitayama.

Response to Arguments

23. Applicant's arguments with respect to claims 1-9, 13-17, 21-24 and 39-49 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date

of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

03/03/2004

NATHAN J. FLYNN
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